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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/521,641	03/08/2000	Adrian Freed	9840-039-999	1451

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EXAMINER	
GRAHAM, ANDREW R	
ART UNIT	**PAPER NUMBER**
2644	16

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/521,641	FREED ET AL.	
	Examiner	Art Unit	
	Andrew Graham	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on April 30, 2004. These drawings are approved by the examiner and have been entered into the application.

Priority

2. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, priority is not granted because the priority document is attributed to five people (Hodes, Hauser, Freed, Wawrzynek, Wessel, listed on page 1), but the present application lists only two of these people as inventors (Hodes, Freed). The present application incorporates the material from the provisional document in its near entirety, and in manner that utilizes substantially identical wording. The record is thus unclear as to which of these people listed on the provisional document should be attributed with the material presented in the present application. For the purpose of the rejections listed below, the priority date of the present application is set at March 8, 2000, which is the filing date of the present application.

It is further noted that this provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for Claims 6-9 and 14-15 of this application. The use of field programmable gate arrays, VLIW processors, RISCs, and Residue Number System processors is not disclosed in the

provisional document in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the provisional application was filed, had possession of the claimed invention set forth by these limitations. The details of the overlap-add technique, as provided in the limitations of Claims 14-15, are also not disclosed in the provisional document in such the requisite manner.

Claim Objections

3. **Claims 16-17** are objected to because of the following informalities:

- Claim 16 recites the equation $X_n = x_{n-1} - E\ x_{n-1} - x_{n-2}$, but the equation listed in the specification, page 8, is $X_n = 2x_{n-1} - E\ x_{n-1} - x_{n-2}$
- Claim 17 recites the equation E=(2^(2-e))*m but the equation listed in the specification, page 9, is E-(2^(2-e))*m

Appropriate correction or clarification is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1-13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point

out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 3, and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included or excluded by the claim language. Claims 1, 3, and 10 are specifically rejected for the recitation of the phrase "Re-Mapping" or "Re-Map". This phrase was introduced in the most recent amendment to the specification, in reference to "this re-mapping of number representation". It is recognized that the meaning of such words must be given their plain meaning unless applicant has provided a clear definition in the specification (MPEP 2111.01). Based on the applicant's remarks, "a defined term 'Re-Mapping' to indicate the particular remapping described in the specification" (page 9, amendment submitted 4/30/04), the record indicates that the applicant intends to associate such a "clear definition" with these phrases. However, the examiner respectfully submits that the specification does not provide a clear definition of such terms. Paragraph 0037 of the substitute specification states that the frequency coefficient representations are re-mapped in two ways, with the employment of an internal exponent and the inversion of the bit representation. Paragraph 0038 teaches the details of the bit inversion and paragraph 0039 teaches the details of the internal exponent. The phrase "this re-mapping" thus does not explicitly define a correlation between the two 'remappings' of the specification and the phrases "Re-Mapping" and "Re-Map" of the claims. Appropriate

correction or clarification is required. Until such a "clear definition" is provided by the applicant, or the desired limitations are explicitly incorporated in the claim language, such terms will be given their plain meanings, or read as they would be interpreted by those of ordinary skill in the art.

Claims 2, 4-9, and 11-13 are rejected to due to their respective dependencies upon Claims 1, 3, and 10.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 16-18** are rejected under 35 U.S.C. 102(a) as being anticipated by Hodes et al ("A fixed-point recursive digital oscillator for additive synthesis of audio", Hodes, T. et al, Acoustics, Speech, and Signal Processing, 1999. ICASSP '99. Proceedings., 1999 IEEE International Conference on; Publication Date: 15-19 March 1999, page(s): 993 - 996, vol.2"). Hereafter, this document will be referred to as "Hodes et al".

On page 993, the bottom of column 2, Hodes et al discloses a general form of an oscillator, using the equation:

$$x_n = 2\cos\left(\frac{2\pi f}{f_s}\right) x_{n-1} - x_{n-2}$$

where f_s is the sampling frequency and $f \in (0, f_s/2)$ is the (constant) desired frequency of oscillation.

This equates to "A recursive digital oscillator generating frequency f lying in the range from zero to one-half of a sampling frequency f_s". Hodes et al then teach a modified version of such a generator, wherein the above formula is rewritten as:

$$\begin{aligned} x_n &= 2\cos(w)x_{n-1} - x_{n-2} \\ x_n &= 2(1-\epsilon/2)x_{n-1} - x_{n-2} \\ x_n &= 2x_{n-1} - \epsilon x_{n-1} - x_{n-2} \end{aligned}$$

i.e., where $\cos w = (1 - \epsilon/2)$.

The last of these equations equates to "$X_n = x_{n-1} - E\ x_{n-1} - x_{n-2}$". The listed "cos w = (1 - E/2)" can be rewritten as, and equates to, "E= 2-2cos(w)". Hodes et al also teaches that the "w" in the above equations equates to "2*pi*f/f_s" (page 994, bottom half of column 1).

Regarding **Claim 17**, Hodes et al teaches that the actual represented value for "E" in the above equations is biased to "E-(2^(2-e))*m" (page 994, final 6 lines of column 1).

Regarding **Claim 18**, Hodes et al teaches that "E" is represented with a sixteen bit unsigned mantissa "m" (page 994, final 6 lines of column 1).

6. **Claims 1-5 and 10-18** are rejected under 35 U.S.C. 102(b) as being anticipated by Hodes ("Recursive Oscillators on a Fixed-Point Vector Microprocessor for High Performance Phase-Accurate Real-Time Additive Synthesis", Research Project, CSD-98-1007, Todd D. Hodes; August 6, 1998). This document will hereafter be referred to as "Hodes". The publication date for this document is August 6, 1998, when the document was made available on the NCSTRL, Networked Computer Science Technical Reports Library.

Regarding **Claim 1**, Hodes teaches that the engine of the system receives a series of frames as input, wherein data included in each frame includes frequency, amplitude, and phase data (bottom of page 4; upper half of page 5). This data corresponds to a representation in the spectral domain, and collectively equates to "receiving digital audio signal frames" and "a frequency coefficient representation". Frames are 50% overlapped with individual amplitude envelopes linearly increasing from zero to a specified peak value during the first overlapped portion of a frame and decreasing to zero from the same peak value during the second portion of the overlapped frame, as is shown in Figure 2.1, which illustrates the processing with frames N-1,N, and N+1 (page 5). The illustrated process overlaps and adds successive oscillators with this peaked, triangular amplitude, the two successive frames closely approximate a single varying frequency, varying amplitude partial

(last paragraph, page 5). This equates to "performing additive synthesis". In the second paragraph of page 6, Hodes discloses a general form of an oscillator, and on page 7 and the top of page 8, Hodes teaches a recast, equivalent equation for such a filter, wherein the recasting involves two instances of representation re-mapping. The effect of utilizing the reformulated oscillator equation for generating the sinusoids of the synthesis process minimizes the perceived error in the lower frequency components of the audio signal (top, page 7). The use of this oscillator and its remapping equates to "forming converted frequency coefficients".

Regarding **Claim 2**, the remapping involves a biased, unsigned exponent involved with an internal floating point format. The exponent in this format represents a necessary right shift correction, and includes a coefficient of 2 that allows the exponent to range from 0 to 4 (first full paragraph, page 7). This exponent equates to "defining said frequency coefficient".

Regarding **Claim 3**, Hodes teaches that the exponent is specifically designed as part of the representation for use with a sixteen-bit multiply, wherein the exponent corresponds to a corrective, variable right shift (final paragraph, page 6 and first full paragraph, page 7). This equates to "specifying said exponent to correspond to a right shift amount necessary".

Regarding **Claim 4**, the recast oscillator is mapped onto the T0, Torrent-0 architecture, which uses 16-bit fixed point arithmetic (second paragraph, page 2, and third paragraph, page

6). This reads on "implemented using a 16-bit fixed point processor".

Regarding **Claim 5**, a related implementation the synthesis algorithm of Hodes is designed for a fixed-point vector microprocessor, such as a Torrent-0 microprocessor incorporated on a SPERT board. Such a device is considered to fall under the broadest reasonable interpretation of a "digital signal processor" (page 4, first paragraph, and pages 17-18).

Regarding **Claim 10**, please refer to the like teachings of Claims 1 and 5, noting the standard context of implementing such processing in a digital architecture.

Regarding **Claim 11**, please refer to the like teachings of Claim 1, noting that the inherent "identification" of inputs to which the stages of shifts or re-mapping are applied.

Regarding **Claim 12**, please refer to the like teachings of Claim 2. Regarding **Claim 13**, please refer to the like teachings of Claim 3.

Regarding **Claim 14**, Hodes teaches a synthesis algorithm that includes an engine arranged to receive an input of overlap-add frames (page 4, bottom). Successions of overlap-add frames are called timbral prototypes and at each instant of time, a timbral prototype is being synthesized as a weighted sum of two constituent frames (page 4, bottom, first para. of page 5). The data of each frame includes fixed frequency, peak, amplitude, and initial phase for each partial in the frame. This frame data and

in the input of such frames equates to "receiving". Successive frames are 50% overlapped with individual amplitude envelopes linearly increasing from zero to a specified peak value during the first overlapped portion of a frame and decreasing to zero from the same peak value during the second portion of the overlapped frame, as is shown in Figure 2.1, which illustrates the processing with frames N-1,N, and N+1 (page 5). This equates to "linearly scaling". The illustrated process overlaps and adds successive oscillators with this peaked, triangular amplitude, the two successive frames closely approximate a single varying frequency, varying amplitude partial (last paragraph, page 5). This equates to "summing".

Regarding **Claim 15**, a 50% overlap is specified (third line, first full paragraph, page 5).

Regarding **Claim 16**, on page 6, the second paragraph, Hodes discloses a general form of an oscillator, using the equation:

$$x_n = 2\cos\left(\frac{2\pi f}{f_s}\right) x_{n-1} - x_{n-2}$$

where f_s is the sampling frequency and $f \in (0, f_s/2)$ is the (constant) desired frequency of oscillation.

This equates to "A recursive digital oscillator generating frequency f lying in the range from zero to one-half of a sampling frequency f_s". At the bottom of page 7, Hodes then

teaches a modified version of such a generator, wherein the above formula is rewritten as:

$$\begin{aligned} x_n &= 2\cos(w)x_{n-1} - x_{n-2} \\ x_n &= 2(1-\epsilon/2)x_{n-1} - x_{n-2} \\ x_n &= 2x_{n-1} - \epsilon x_{n-1} - x_{n-2} \end{aligned}$$

i.e., where $\cos w = (1-\epsilon/2)$.

The last of these equations equates to "$X_n = x_{n-1} - E\ x_{n-1} - x_{n-2}$". The listed "cos w = (1 - E/2)" can be rewritten as and equates to "E= 2-2cos(w)". A comparison between the equation of Page 6 and the first equation of Page 7 shows that the "w" in the above equations equates to "$2*pi*f/f_s$".

Regarding **Claim 17**, Hodes 1 teaches that the actual represented value for "E" in the above equations is biased to "E-(2^(2-e))*m" (first full paragraph, page 7).

Regarding **Claim 18**, Hodes et al teaches that "E" is represented with a sixteen bit unsigned mantissa "m" (first full paragraph, page 7).

7. **Claims 14-15** are rejected under 35 U.S.C. 102(b) as being anticipated by McAulay et al (USPN 47937873). Hereafter, "McAulay et al" will be referred to as "McAulay".

McAulay teaches a computationally efficient sine wave synthesis system for processing acoustic waveforms. The system is based on Fast-Fourier Transform overlap-and-add techniques (col. 4, lines 6-13). The successive frames each include sine

wave parameters, including amplitude, frequency, and phase information (col. 7, lines 1-7). These frame representations, in view of their reception into the receiver section (16), read on "receiving a sequence". Figure 1 illustrates the overlap and add technique, for exemplary frames K and K+1 (col. 5, lines 65-68). Triangular windows A and B are applied to the frames, which are overlapped in a region c (col. 5, line 68 and col. 6, lines 1-7). This application of a triangular window reads on "linearly scaling". The amplitude, frequency, and phase value of successive frames are then summed and divided by two, thereby providing approximations of a sinusoid at a midpoints between the frames (col. 6, lines 21-51). This equates to "summing successive scaled frame partials" and the midpoint approximation equates to "approximating a varying frequency varying-amplitude frame partial".

Regarding **Claim 15**, an exemplary sampling rate is given as 20 ms, though the triangular windows are 40 ms wide (col. 6, lines 10-18). This, in view of the illustration of Figure 1, reads on "approximately 50% overlap between each pair of said summed partials".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1-5, and 10-13** are rejected under 35 U.S.C. 103 (a) as being unpatentable over Wei (USPN 6029133) in view of Kunimoto (JP 03-125513).

Wei discloses a synthesizer that recursively derives frames of waveforms. The system provides the pitch frequency (45) for each audio frame as well as the magnitude (60), time durations of each frame (55), and ending phase (50) to second order resonators (40) that generate the corresponding harmonics, which are then summed and shaped by a gain circuit (70) according to an input description of the original audio signal (col. 3, lines 14-24 and col. 5, lines 22-65). Figures 2a and 2b illustrate the recursive structure of the digital oscillators (col. 5, lines 31-62). These devices, and the combination of their outputs read on "A method of performing additive synthesis of digital audio signals in a recursive digital oscillator". As can be seen in Figure 1, the inputs for the system include the pitch frequency (15) for the current synthesizing frame, the ending phase information (25) for the harmonics in each frame, and the magnitudes (35) of each of the harmonics in each frame (col. 3, line 67 and col. 4, lines 1-14). This information as

input reads on "receiving digital audio signal frames wherein each digital audio signal frame includes a set of frequency, amplitude, and phase components represented as coefficients of variables in a mathematical expression". The merging of the waveforms reads on "performing additive synthesis with said converted frequency coefficients" (col. 7, lines 46-54).

While Wei discloses the general structure synthesizing the digital waves, Wei does not specify:

- that the frequency coefficients are linearly remapped to bias audio reproduction accuracy toward low frequency signals

Kunimoto teaches a filter for use in musical tone synthesis. The system processing includes a multiplication in terms of a fixed decimal point, and bit shifting in view of an exponent part of a coefficient ("Purpose"). A coefficient is applied to an input signal, D, through the use of a multiplier (21) and an exponent part of the coefficient is supplied to a bit shifter (22) as the quantity of a negative bit shift to be applied to the received signal ("Constitution" and Figure 2). The effect of these operations is disclosed as being to improved the resolution of the low frequency part of the inputted signal (last line, "Constitution"). The application of this filter to a received signal reads on "forming converted frequency coefficients by Re-Mapping of bits of said frequency coefficient

representation to bias audio reproduction accuracy toward low frequency signals".

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to include the bit filter of Kunimoto as part of the recursive digital filter of Wei. The motivation behind such a modification would have been that the system of Kunimoto would have improved the resolution of the low frequencies of a signal.

Regarding **Claim 2**, Kunimoto teaches that the applied coefficient is processed in terms of a floating method, and that the exponent part of the coefficient designates the amount of negative phase shift to be applied to the received signal for improving low frequency resolution. This reads on "defining said frequency coefficient representation with an exponent characterizing a floating point range extension".

Regarding **Claim 3**, Kunimoto teaches that the exponent part of the applied coefficient corresponds to a negative shift for the received signal, and that the inputted signal is of a prescribed length, such as 16 bits. Collectively, this teachings, in regards to the bit representation of the input signal, reads on "introduced by limiting re-mapping coefficients to 16 bits".

Regarding **Claim 4**, both Wei and Kunimoto disclose the use of components that process digital signals. Kunimoto teaches that the input signal is processed by way of a fixed decimal

point, and that the input signal is of a prescribed length, such as 16 bits. This reads on "a 16-bit fixed point processor".

Regarding **Claim 5**, the components (21,22) of Kunimoto processes a digital signal of a prescribed length, such as 1 bits. Wei also teaches that a variety of methods that are known in the art for computing sinusoids with DSPs (col. 2, lines 20-22). This, in view of the broadest reasonable interpretation of such a limitation, collectively reads on "utilizing a digital signal processor".

Regarding **Claim 10**, please refer to the like teachings of Claims 1 and 5, noting the context of the implementation of such systems disclosed by Wei.

Regarding **Claim 11**, please refer to the like teachings of Claim 1, and the inherent "identification" of inputs received in the system of Wei.

Regarding **Claim 12**, please refer to the like teachings of Claim 2. Regarding **Claim 13**, please refer to the like teachings of Claim 3.

9. **Claims 6-8** are rejected under 35 U.S.C. 103 (a) as being unpatentable over Wei in view of Kunimoto as applied above, and in further view of Dowling (USPN 6163836).

As detailed above, Wei discloses a recursive digital oscillator, and Kunimoto teaches a filter that improved the low frequency resolution of a processed signal. Both Wei and

Kunimoto disclose the use of components that process digital signals.

However, Wei in view of Kunimoto do not specify:

- that the processor is a field programmable gate array

Dowling discloses a processor with programmable addressing modes. One particular embodiment of the system of Dowling is a field programmable gate array (col. 15, lines 12-21). Such a processor involves the advantages of a hardware description language code that is used for both verification and implementation, as well as special circuitry to implement common arithmetic functions Col. 16, lines 32-49). This embodiment reads on "implemented utilizing a field programmable gate array".

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to execute the synthesis system of Wei in view of Kunimoto on the processor of Dowling. The motivation behind such a modification would have been the use of the same description language code and the specialized circuitry as taught by Dowling.

Regarding **Claim 7**, another embodiment of the system of Dowling is a Very Long Instruction Word processor, which reads on "implemented using a Very Long Instruction Word processor" (col. 17, lines 20-65).

Regarding **Claim 8**, Dowling also discloses the use and known advantages of Reduced Instruction Set Computers, the

incorporation of which reads on "implemented utilizing a Reduced Instruction Set Computer" (col. 1, lines 21-65).

10. **Claim 9** is rejected under 35 U.S.C. 103 (a) as being unpatentable over Wei in view of Kunimoto as applied above, and in further view of Capps et al (USPN 4910699). Hereafter, "Capps et al" will simply be referred to as "Capps".

As detailed above, Wei discloses a recursive digital oscillator, and Kunimoto teaches a filter that improved the low frequency resolution of a processed signal. Both Wei and Kunimoto disclose the use of components that process digital signals.

However, Wei in view of Kunimoto do not specify:

- that the processor is a Residue Number System processor

Capps discloses an optical computer that includes binary to residue conversion and deconversion. Optical computers are disclosed as being readily supportive of complex global interconnect structures, while their electronic counterparts are not (col. 4, lines 56-68 and col. 5, lines 1-2). Capps also discloses that residue number processing more optimally matches optical technology, and significant processing speeds may potentially be obtained wit such systems (col. 5, lines 10-18). The system of Capps includes binary to residue converter (2) to enable residue number processing of binary data using optical processors, and residue to binary converters for converting the

data back to a more local, universal binary form (Figure 1). This processor reads on "implemented utilizing a Residue Number System processor.

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to utilize the optical processor and converters of Capps in the system of Wei in view of Kunimoto. The motivation behind such a modification would have been the enhanced processing speed provided by the parallel optical processors, and the conversion means that would have enabled the input and outputs of the system to be in the more common and therefore prominently useful binary format.

Response to Arguments

11. On page 10, lines 1-3, the applicants have respectfully submitted that "applying this specific term to claims 1-13 renders all such limitations patentably distinct from the prior art". The examiner respectfully submits that the amended version of the claims is indefinite, as is discussed above in regards to the rejections made under 35 U.S.C. 112. It is further noted that new references, Kunimoto and Hodes, have been separately applied to these claims, as was necessitated by such an amendment.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Graham whose telephone number is (703) 308-6729. The examiner can normally be reached on Monday-Friday (7:30-4:30), excluding alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Isen, can be reached at (703) 305-4386. The fax number for the organization where this application or proceeding is assigned is 703-872-9314

for regular communications, and 703-872-9315 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

AG
Andrew Graham
Examiner
A.U. 2644

ag
July 12, 2004

FORESTER W. ISEN
SUPERVISORY PATENT EXAMINER